

REMARKS

Consideration of the application as preliminarily amended is respectfully requested.

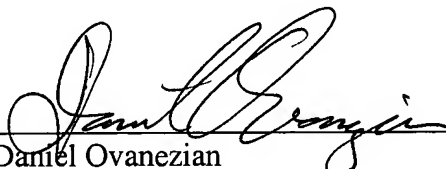
The specification has been amended to correct minor matters of form. Figure 11B was improperly labeled as Figure 11C in the Brief Description of the Drawings on page 7 of the application. It is respectfully submitted that no new matter has been introduced by this preliminary amendment.

If there are any additional charges, please charge them to our Deposit Account No. 02-2666.

Respectfully submitted,

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[0020] **FIG. 8** illustrates one embodiment of a larger size stage-1 scalable non-blocking switching network.

[0021] **FIG. 9** illustrates one embodiment of a stage-1 scalable non-blocking switching network with sixteen M conductors.

[0022] **FIG. 10** is a block diagram illustrating one embodiment of a stage-2 scalable non-blocking switching network (2-SN) and a circuit with four logic circuits of **FIG. 1**, each using the scalable non-blocking switching network of **FIG. 9**.

[0023] **FIG. 11A** illustrates a block diagram embodiment of the stage-2 scalable non-blocking switching network of **FIG. 10**.

[0024] **FIG. 11C** illustrates one embodiment of the first part of the stage-2 scalable non-blocking switching network of **FIG. 11A**.

[0025] **FIG. 12** illustrates one embodiment of a stage-1 scalable non-blocking switching network implementing the second part of the 2-SN of **FIG. 11A**.

(O[0-3]) of the CLST4 100 circuit of FIG. 1. The expansion exponent R is again 1.0 in this circuit 1000.

[0050] The use of scalable non-blocking switching networks in this next level of circuit hierarchy, connecting large number of conductors to multiple sets of conductors, is illustrated in FIG. 11A. FIG. 11A illustrates an embodiment, in block diagram form, of circuit MTX16 1050 of FIG. 10 where the sixty four M conductors 1101 (M[0-47], OW[0-7], OE[0-7]) correspond to conductors 1055 and 1056 of FIG. 10. The first stage of intermediate conductors is composed of N0 (where N0=4) sets of sixteen IO<sub>i</sub> conductors (where IO<sub>i</sub> = M/N0 = 16 for i = [1-N0]) 1150, 1160, 1170, and 1180. The M conductors 1101 interface to the first four sets of intermediate stage IO<sub>i</sub> conductors 1150, 1160, 1170, 1180 using the switches of sub-networks 1110, 1120, 1130 and 1140. FIG. 11B illustrates a scheme where conductors 1101 connects to conductors 1160 through sub-network 1120. The connection scheme where conductors 1101 connect to conductors 1150 through sub-network 1110, and to conductors 1170 through sub-network 1130, and to conductors 1180 through sub-network 1140 are the same as sub-network 1120 of FIG. 11B. The number of switches used between the M conductors 1101 to the four sets of first stage intermediate conductors 1150, 1160, 1170, 1180 in this embodiment is MxN0=256. As described in relation to FIG. 5, an alternative implementation is to have (M-N0+1) x N0 switches instead.

[0051] FIG. 12 illustrates an embodiment of circuit TA1 1165 where conductors 1160 is the second N0 set of IO<sub>i</sub> conductors, where i=2 and IO<sub>i</sub> = 16; intermediate conductors 1201-1216 (which correspond to conductors 1160 of FIG. 11A) interface to

**FIG. 10** has a reduction in the number of switches by the difference between  $N \times M = 16M$  and  $(N_0+N_1) \times M = (4+4) \times M = 8M$ ; the 3-SN and 4-SN where  $(N_0+N_1+N_2) = (2+2+4) = 8$  and  $(N_0+N_1+N_2+N_3) = (2+2+2+2) = 8$ , respectively, has no improvement over the 2-SN where  $(N_0+N_1) = (4+4) = 8$ . As such, it may make sense only when the sum of  $N_i$ , the number of sets of the intermediate conductors for each stage, add up to be less than the previous stage multi-stage SN. Thus, it can be seen that for  $N=64$ , a 3-SN using  $N_0=N_1=N_2=4$  where  $(N_0+N_1+N_2) = 12$  would be very effective in switch reduction over a 2-SN using  $N_0=N_1=8$  with  $(N_0+N_1) = 16$  and similarly for the 2-SN over 1-SN where  $N=64$ .

[0057] Thus we have described two levels of circuit hierarchy using scalable non-blocking switching networks where sixty four  $M$  conductors fan in to connect, through a 2-SN and then a 1-SN, to sixteen four-input logic cells. Sixteen of the sixty four  $M$  conductors are directly connected to the sixteen outputs of each of the four CLST4 (125-128 of 100 in **FIG. 1**) circuits, providing unrestricted connections from any output to all sixteen logic cells. The first level of circuit hierarchy includes the circuit CLST4 100 of **FIG. 1** with MTX 200 implemented as the 1-SN 900 of **FIG. 9** where CLST4 100 has four four-input logic cells 10-40 and two flip-flops 50, 60 as shown in **FIG. 1**. The next higher second level of circuit hierarchy is the CLST16 1000 circuits of **FIG. 10** having four CLST4 100 circuits with a 2-SN MTX16 1050 as shown in **FIG. 10**, where the network 1050 implementation is illustrated in **FIG. 11A**, **FIG. 11B** and **FIG. 12**. In CLST16 1000, each of sixteen outputs 1065, 1075, 1085, 1095 (connecting directly to conductors 1056) has unrestricted connectivity to every logic cell in the CLST16 1000